

In the Claims:

The following listing of Claims replaces all previous listings:

1. (Currently amended) An integrated circuit structure comprising:
an isolation structure that electrically isolates an active region of an integrated circuit substrate from adjacent active regions;
an insulation layer extending from the isolation structure to beneath the active region;
and
an epitaxial silicon layer that extends from the active region through the insulation layer to a substrate beneath the insulation layer, wherein the insulation layer comprises a trench thermal oxide layer on an inner side wall of a trench in the substrate, the insulation layer extending through the inner side wall of the trench to beneath the active region.

Claim 2 (Canceled).

3. (Previously presented) An integrated circuit structure according to Claim 1 wherein the isolation structure further comprises:
a nitride liner on the trench thermal oxide layer;
a field oxide layer in the trench on the nitride liner.

4. (Previously presented) An integrated circuit structure according to Claim 3 wherein the nitride liner extends through the inner side wall into the insulation layer beneath the active region.

5. (Original) An integrated circuit structure according to Claim 1 further comprising:
an impurity-doped region at an interface of the substrate and the epitaxial silicon layer.

Claim 6 (Canceled).

7. (Original) An integrated circuit structure according to Claim 1 wherein the active region comprises a strained silicon crystalline structure.

8. (Currently amended) An integrated circuit structure according to Claim [[2]] 1 wherein the epitaxial silicon layer comprises a first epitaxial silicon layer in the active region adjacent to and in contact with the inner side wall of the trench, the structure further comprising:

a second epitaxial silicon layer in the active region spaced apart from the first epitaxial silicon layer.

Claims 9-21 (Canceled).

22. (Currently amended) An integrated circuit structure comprising:
an isolation structure that electrically isolates an active region including a plurality of gates from adjacent active regions; [[and]]

an epitaxial silicon layer in the active region between at least two of the plurality of gates extending from the active region to a substrate beneath the active region;

a first insulation layer extending from opposing portions of the isolation structure to beneath the plurality of gates; and

a second insulation layer extending from opposing portions of the isolation structure to beneath the first insulation layer, wherein the epitaxial silicon layer extends through the second insulation layer.

23. (Previously presented) An integrated circuit structure according to Claim 22 wherein the epitaxial silicon layer comprises a first epitaxial silicon layer, the structure further comprising:

second and third epitaxial silicon layers in the active region between the isolation structure and the plurality of gates and extending from the active region to the substrate.

Claims 24-25 (Canceled).

26. (Previously presented) An integrated circuit structure according to Claim 22 further comprising: a nitride liner beneath the plurality of gates.

Claims 27-30 (Canceled).